Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	1	((redundant redundanc$3)near5(latch$3 register FF flip-flop)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 logic near10 output near10 active	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/13 18:47
L2	1	((redundant redundanc$3)near5(latch$3 register FF flip-flop)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 logic near10 output near10 exclu$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/13 18:46
L1	4	((redundant redundanc$3)near5(latch$3 register FF flip-flop)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 logic and output	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/13 18:43
S64 6	23	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/13 18:33
S64 5	619	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/13 10:04
S64 4	39	(((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 select$3 adj2 logic)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/13 10:04

S64 3	1	(((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 select$3 adj2 logic) and 716/6.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/13 09:56
S64 2	1	(((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 select$3 adj2 logic) and 716/10.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/13 09:55
S64 1	1	(((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and add$3 adj2 select$3 adj2 logic).clm.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/13 09:53
S64 0	0	(((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition and adding adj selecting adj logic).clm.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/12 22:09
S63 9	1	(((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and (clock adj cycle) and transition).clm.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/12 21:59
S21 3	11	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/12 21:51
S63 7	1271	716/6.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 21:37

S63 6	918	716/10.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 21:37
S27 0	3	(redundant redundanc$3)adj2(latch$3) and (clock adj cycle) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/01/12 21:17